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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,763	10/15/2003	Sherman H. Yip	SUNMP360	1971

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EXAMINER	
WANG, BEN C	

ART UNIT	PAPER NUMBER
2196	

DATE MAILED: 12/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,763	YIP ET AL.	
	Examiner	Art Unit	
	Ben C. Wang	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending in this application and presented for examination.

Claim Rejections – 35 USC § 102(e)

2. The following is a quotation of 35 U.S.C. 102(e) which forms the basis for all obviousness rejections set forth in this office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 9, 13-15, and 21 are rejected under 35 U.S.C. 102(e) as being unpatentable over Wygodny et al. (hereafter 'Wygodny') (*US Patent No. 7,058,928 B2).*

4. **As to claim 1**, Wygodny discloses defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction (Fig. 5, elements 502, 504, *CfireWnd::GetBitmapSize* is defined in element 502 (highlighted portion) and is shown in element 504; Fig. 6; Fig. 7; Fig. 8; Col. 3, lines 32-38, lines 57-59; Col. 3, line 65 through Col. 4, line 1; Col. 4, lines 48-58; Col. 13, lines 37-47, lines 49-53); tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components (Fig. 3A, elements 334, 318, 380; Col. 4, lines 41-42; Col. 9, lines 41-49); and displaying a progression of each of the plurality

of graphical icons through the one or more hardware components during the execution of code segment (Col. 3, lines 25-30, lines 59-64; Col. 8, lines 8-12).

5. **As to claim 13**, Wygodny discloses program instructions for defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction (Fig. 5, elements 502, 504, *CfireWnd::GetBitmapSize* is defined in element 502 (highlighted portion) and is shown in element 504; Fig. 6; Fig. 7; Fig. 8; Col. 3, lines 32-38, lines 57-59; Col. 3, line 65 through Col. 4, line 1; Col. 4, lines 48-58; Col. 13, lines 37-47, lines 49-53); program instructions for tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components (Fig. 3A, elements 334, 318, 380; Col. 4, lines 41-42; Col. 9, lines 41-49); and program instructions for displaying a progression of each of the plurality of graphical icons through the one ore more hardware components during the execution of the code segment (Col. 3, lines 25-30, lines 59-64; Col. 8, lines 8-12).

6. **As to claims 2 and 14**, Wygodny discloses that the plurality of instructions define a group of instructions (Fig. 5, elements 502, 504, *CfireWnd::GetBitmapSize* is defined in element 502 (highlighted portion) and is shown in element 504; Fig. 6; Fig. 7; Fig. 8; Col. 3, lines 32-38, lines 57-59; Col. 3, line 65 through Col. 4, line 1; Col. 4, lines 48-58; Col. 13, lines 37-47, lines 49-53), and each instruction in the group of

instructions being processed in order defined by the code segment (Fig. 3A, elements 334, 318, 380; Col. 4, lines 41-42; Col. 9, lines 41-49).

7. **As to claims 3 and 15**, Wygodny discloses processing the group of instructions (Fig. 3A, elements 334, 318, 380; Col. 4, lines 41-42; Col. 9, lines 41-49); and enabling display a member of the group (Col. 3, lines 25-30, lines 59-64; Col. 8, lines 8-12).

8. **As to claims 9 and 21**, Wygodny discloses that each graphical icon is associated with a specific instruction (Fig. 5, elements 502, 504, *CfireWnd::GetBitmapSize* is defined in element 502 (highlighted portion) and is shown in element 504; Fig. 6; Fig. 7; Fig. 8; Col. 3, lines 32-38, lines 57-59; Col. 3, line 65 through Col. 4, line 1; Col. 4, lines 48-58; Col. 13, lines 37-47, lines 49-53).

Claim Rejections – 35 USC § 103(a)

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4-8, 11, 16, 19-20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wygodny in view of Austin et al. (hereafter 'Austin') (*SimpleScalar: An Infrastructure for Computer System Modeling, Feb. 2002, IEEE*).

11. **As to claims 4 and 16**, Wygodny discloses that each graphical icon is associated with a specific instruction (Fig. 5, elements 502, 504, *CfireWnd::GetBitmapSize* is defined in element 502 (highlighted portion) and is shown in element 504; Fig. 6; Fig. 7; Fig. 8; Col. 3, lines 32-38, lines 57-59; Col. 3, line 65 through Col. 4, line 1; Col. 4, lines 48-58; Col. 13, lines 37-47, lines 49-53).

But, Wygodny does not disclose the method operation of displaying the progression of each of the plurality of instructions includes, displaying a tabular view of the progression of each of the plurality of instructions through the one or more hardware components during the execution of the code segment.

However, in an analogous art, Austin discloses the method operation of displaying the progression of each of the plurality of instructions includes, displaying a tabular view of the progression of each of the plurality of instructions through the one or more hardware components during the execution of the code segment (Fig 1, middle area; Sec. of Modeling With SimpleScalar, 4th paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Austin to further provide the method operation of displaying the progression of each of the plurality of instructions includes, displaying a tabular view of the progression of each

of the plurality of instructions through the one or more hardware components during the execution of the code segment in Wygodny system.

The motivation is to further provide an infrastructure for computer hardware system simulation and architectural modeling in Wygodny system ([Austin], Summary).

12. **As to claims 7 and 19**, Wygodny system does not disclose that the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color.

However, in an analogous art, Austin discloses that the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color (Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Austin to further provide the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color in Wygodny system.

The motivation is to further provide an infrastructure for computer hardware system simulation and architectural modeling in Wygodny system ([Austin], Summary).

13. **As to claims 8 and 20**, Wygodny does not disclose that the progression is movement between the one or more hardware components through intervals of time.

However, in an analogous art, Austin discloses that the progression is movement between the one or more hardware components through intervals of time (Fig. 1; Sec. of Modeling With SimpleScalar, 4th paragraph, lines 1-3).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Austin to further provide the progression is movement between the one or more hardware components through intervals of time in Wygodny system.

The motivation is to further provide an infrastructure for computer hardware system simulation and architectural modeling in Wygodny system ([Austin], Summary).

14. **As to claims 11 and 23**, Wygodny does not disclose that the execution of the code segment generates the instructions to the one or more hardware components.

However, in an analogous art, Austin discloses that the execution of the code segment generates the instructions to the one or more hardware components (Fig 1, left area, middle area; Sec. of Modeling With SimpleScalar, 4th paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Austin to further provide that the execution of the code segment generates the instructions to the one or more hardware components in Wygodny system.

The motivation is to further provide an infrastructure for computer hardware system simulation and architectural modeling in Wygodny system ([Austin], Summary).

15. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wygodny in view of Austin and further in view of Wong et al. (hereafter 'Wong') (*US Patent No. 6,175,364 B1*).

16. **As to claims 5 and 17**, Wygodny and Austin do not disclose selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons.

However, in an analogous art, Wong discloses selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons (Col. 1, lines 22-31).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and Austin with the teachings of Wong to further provide selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons in Wygodny-Austin system.

The motivation is to provide end-users for visualizing relatively large amounts of data in a limited display space ([Wong], Col. 2, lines 34-37).

17. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wygodny in view of Austin and Wong and further in view of Drongowski et al (hereafter 'Drongowski') (*Profiling to Tune C Programs on Alpha, April 6, 2001, Hewlett Packard Company*).

18. **As to claims 6 and 18**, Wygodny, Austin, and Wong do not specifically disclose that the information is defined by one or more of a name of the instruction, an internal representation of the instruction, a program counter associated with an instruction, a physical memory location of the instruction, an instruction disassembly, a register source, a register destination, a virtual addresses of data, and a physical address of the data to be loaded.

However, in an analogous art, Drongowski discloses that the information is defined by one or more of a name of the instruction (P. 23, Alpha no-op Instructions, Mnemonic), an internal representation of the instruction (P. 26, bottom area, 0x120001190), a program counter associated with an instruction (P. 26, bottom area, :count), a physical memory location of the instruction (P. 32, 0x120001150 for example), an instruction disassembly (P. 23, Alpha no-op Instructions, Disassembly), a register source (P. 23, Alpha no-op Instructions, Mnemonic, Rx for example), a register destination (P. 23, Alpha no-op Instructions, Mnemonic, R31 for example), a virtual addresses of data (P. 33, Sec. 5.4.3), and a physical address of the data (P. 33, Sec. 5.4.3) to be loaded.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny, Austin, and Wong with the teachings of Drongowski to further provide performance tuning mechanism for Wygodny-Austin-Wong system.

The motivation is to provide performance tuning to identify and remove bottleneck ([Drongowski], Sec. 1.0).

19. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wygodny in view of Hollingsworth et al. (hereafter 'Hollingsworth') (*The Clipper Processor: Instruction Set Architecture And Implementation, February 1989, ACM*) and further in view of Sherwood et al. (hereafter 'Sherwood') (*A Pipelined Memory Architecture for High Throughput Network Processors, June 2003, IEEE*).

20. **As to claims 10 and 22**, Wygodny does not disclose that the one or more hardware components is defined by one or more of an instruction buffer, an integer instruction execution pipeline, a loads and stores execution pipeline, a branch execution pipeline, a floating point add execution pipeline, a floating point multiply execution pipeline, a microprocessor, an address switch, a data switch, a memory controller, an Ethernet, a network, a data cache, a memory, a bus, an interconnect, a motherboard routing, and a protocol.

However, in an analogous art, Hollingsworth discloses that the one or more hardware components is defined by one or more of an instruction buffer (Sec. of Bit Ordering, 2nd paragraph, lines 5-10; Sec. of Instruction Bus Interface, 1st paragraph, lines 1-5; Fig. 4, entity of Instruction Bus Interface, Instruction Buffer), an integer instruction execution pipeline (Fig. 4, entity of Integer Execution Unit; Fig. 6, entity of Integer Execution Unit), a loads and stores execution pipeline (Sec. of Motivation and

Design Philosophy, 4th paragraph, lines 7-13; Sec. of INSTRUCTION FORMATS AND ADDRESSING MODES, Addressing Modes, 1-11), a branch execution pipeline (Sec. of Branches and Condition Codes; Table III, Branch Logic), a floating point add execution pipeline (Fig. 4, entity of Floating Point Execution Unit; Fig. 5, entity of Floating Point Unit; Fig. 6, entity of Floating Point Execution Unit), a floating point multiply execution pipeline (Fig. 4, entity of Floating Point Execution Unit; Fig. 5, entity of Floating Point Unit; Fig. 6, entity of Floating Point Execution Unit), a microprocessor (Fig. 1, entity of CPU/FPU), an address switch (1st Sec., 1st paragraph, lines 10-20), a data switch (1st Sec., 2nd paragraph, lines 1-11; Sec. of Address Space), a memory controller (Sec. of Memory Architecture and Data Types, Memory Architecture), a data cache (1st Sec., 1st paragraph, lines 1-5; Sec. of Caching), a memory (Fig. 1, entity of MAIN MEMORY), a bus (Fig. 5, entity of Instruction Bus Interface, Instruction Bus to I-CAMMU, entity of Data Bus Interface, Data Bus to D-CAMAU; Fig. 1, entity of CLIPPER BUS; Sec. of Data Bus Interface), an interconnect (Fig. 5, bold arrow lines; Table III, Other - Interconnect), and a protocol (Sec. of Tradeoffs And Extensions, Better Multiprocessor Cache Consistency, lines 1-5).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Hollingsworth to further provide those hardware components in Wygodny system.

The motivation is to provide high performance, cost effectiveness, convenient programmability, and an architecture that can be expanded as technology improvise

and the an of computer architecture design advances ([Hollingsworth], Sec. of Conclusions).

Furthermore, Wygodny and Hollingsworth do not disclose an Ethernet, a network, a motherboard routing.

However, in an analogous art, Sherwood discloses that a network (Fig. 1; Sec. 3), a motherboard routing (Fig. 2; Fig. 3; Sec. 2.1; Sec. 2.2). Official Notice is taken that an Ethernet is well known in the art.

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and Hollingsworth with the teachings of Sherwood to further provide routing and networking components in Wygodny-Hollingsworth system.

The motivation is to provide a programmable and scalable network processor solution for next generation backbone routers ([Sherwood], Sec. of Summary).

21. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wygodny in view of Hollingsworth.

22. **As to claims 12 and 24**, Wygodny does not disclose that the plurality of instructions of the code segment are defined by one or more of a load instruction, an add instruction, a subtract instruction, a store instruction, a branch instruction, a register movement instruction, a shift instruction, an input instruction, and an output instruction.

However, in an analogous art, Hollingsworth discloses that the plurality of instructions (Table II. Operations and Opcodes, Instruction Type, Variants and Op Codes) of the code segment are defined by one or more of a load instruction (LOAD), an add instruction (ADD), a subtract instruction (SUBTRACT), a store instruction (STORE), a branch instruction (BRANCH CONDITIOANL; BRANCH FLOATING EXCEPTION), a register movement instruction (SAVE REGISTERS; RESTORE REGISTERS), a shift instruction (SHIFT ARITHMETIC; SHIFT LOGICAL), an input instruction (LOAD address(loada); LOAD byte(loadb)), and an output instruction STORE word(storw); STORE byte(storb)).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Wygodny and the teachings of Hollingsworth to further provide those instructions in Wygodny system.

The motivation is to provide an instruction set for convenient and efficient programmability, and it can be easily implemented in hardware ([Hollingsworth], Sec. of Instruction Set).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on 571-272-2333. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BCW

November 27, 2006

N. El-Hady

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SUPERVISORY PATENT EXAMINER